Amendments to the Specification:

Please replace the paragraph beginning on page 3, line 13, with the following:

In the solution represented in Figure 3, the current instruction contained in the register IR and the flags F converge towards an address generator AG. The address generator AG operates under the control of a sequencer S, which is clocked by the clock signal CLK and at which there arrive the signals from the system bus SB. The addresses generated by the generator AG reach a microprocessor MPC, the operation of which evolves under the control of an incremental signal INCR coming from the sequencer ~~R~~ S. The microprocessor MPC co-operates with a memory MCS, commonly referred to as control memory, in which a microprogram is stored, which defines the sequences of the control signals of the finite state machine. The output from the control memory CS drives a further circuit CB/D, which functions as control buffer/decoder. The circuit CB/D generates the control signals CS that are to be sent to the CPU. In the diagram of Figure 3, there is also visible an internal address bus, designated by IAB, as well as a line EEF.

Please replace the paragraph beginning on page 7, line 21, with the following:

Basically, the solution described here envisages duplication of the control unit in the two units UC0 and UC1. The first unit in question, *i.e.*, the unit UC0, is of the hardwired type, *i.e.*, with a definitively fixed structure, according to the criteria commonly adopted in the prior art. Instead, the unit UC1 is programmable and hence flexible. Programming of the latter unit is performed by the unit UC0 by means of appropriate instructions, in practice with a memory-programming operation. For this reason, the programming instruction is included in the [[th]] basic instruction set.

Please replace the paragraph beginning on page 8, line 17, with the following:

In the aforesaid idle state, the respective output lines corresponding to the signal CS1 are kept at "0." In the table of Figure 5, there are comprised altogether 2^{n+k+j} allowed states for the possible machine. Each state is represented by a sequence of j + m bits, in which the first

j bits (NS1) identify the next state, whilst the last ~~n~~ m bits (CS1) correspond to the corresponding output signal.